REMARKS/ARGUMENTS

Information Disclosure Statement

Applicant submitted an Information Disclosure Statement (IDS) on 12/15/2004 in relation to the present application. A copy of the original IDS and accompanying transmittal letter are attached. Thus far in the prosecution of the present application, the Examiner has not indicated that she has considered the references contained in the IDS. Applicant respectfully requests the Examiner to include in the next Office Action an initialed version of the IDS indicating the Examiner has considered the references contained in the IDS.

In the Office Action, the Examiner noted that claims 1-63 are pending in the application. The Examiner additionally stated that claims 1-63 are rejected. By this amendment, claims 1-63 have been cancelled and new claims 64-74 have been added. Hence, claims 64-74 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Applicant has canceled all the original and previously presented claims. Applicant respectfully asserts the newly added claims are not anticipated nor obviated by the references cited by the Examiner in the Office Action. Applicant notes the Examiner rejected claims 8 and 9 under 35 U.S.C. 103(a) as being unpatentable over Hoyt et al., U.S. Patent No. 5,604,877 (herein after *Hoyt*) in view of Brown et al., U.S. Patent No. 5,867,701 (hereinafter *Brown*). Applicant makes the following arguments to point out

the specific distinctions believed to render the newly presented claims patentable over the cited references.

Brown discloses a deeply pipelined microprocessor having a front-end of early pipeline stages, namely instruction fetch and decode stages, and a back-end of late pipeline stages, namely instruction execution and retirement stages. The front-end fetches x86 macroinstructions and decodes them into a sequence of micro-operations (uops) that the back-end executes and retires. The microprocessor performs speculative execution of instructions. That is, when the front-end encounters a branch instruction, the front-end predicts whether the branch instruction will be taken or not taken. If the branch instruction is predicted not taken, then the front-end begins to fetch and decode instructions in the sequential path immediately after the branch instruction will be executed; however, if the branch instruction is predicted taken, then the front-end begins to fetch and decode instructions in the target path specified by the branch instruction target address. The instructions in the selected path are said to be speculatively executed, since if the prediction was incorrect the instructions in the selected path must be flushed from the pipeline before they are retired to update the architectural state of the microprocessor.

The front-end may recognize certain fault conditions or events related to the fetched and decoded macroinstructions; however, the fault conditions or events cannot be acted upon until the back-end because the microprocessor may be speculatively executing the macroinstruction causing the fault condition. Consequently, it is possible that the macroinstruction causing the fault condition will be flushed and never retired. Therefore, the microprocessor must only generate the architected fault if the macroinstruction causing the fault condition actually reaches the retirement stages of the back-end. This requirement makes it difficult to maintain precise timing of the x86 architecture fault model in such a complex and deeply pipelined processor.

To solve this problem, *Brown* is directed to a mechanism for the front-end to detect fault conditions or events and in response to insert supplemental uops into the normal uop flow to communicate the fault conditions or events to the back-end. One of the fault

conditions the front-end recognizes is that the currently executing program includes a macroinstruction containing an invalid opcode, which in the x86 architecture fault model requires the generation of an Invalid Opcode fault. If the front-end detects a macroinstruction with an invalid opcode, the front-end inserts a supplemental invalid opcode uop into the normal uop flow. If the supplemental invalid opcode uop reaches the retirement stages of the back-end without being flushed (i.e., there was no branch instruction misprediction), then the back-end generates an architected Invalid Opcode fault in response to the communication from the front-end.

Notably, the microprocessor taught in *Brown* detects a macroinstruction having an invalid opcode expressly for the purpose of generating an architected Invalid Opcode fault to indicate there is an error in the currently executing program. In particular, the microprocessor taught in *Brown* does not detect a macroinstruction having an invalid opcode for the purpose of detecting that a branch predictor of the microprocessor has mispredicted a branch instruction. In contrast, the present invention defined by the new claims is directed to a microprocessor that detects a misprediction by a BTAC of a previously executed branch instruction by detecting that a byte in a cache line in the instruction stream which the BTAC branch history predicted was an opcode byte of a previously executed branch instruction is no longer an opcode byte of the instruction currently at the location in the cache line, such condition as may be caused by self-modifying code or virtual aliasing, for example.

Finally, Applicant respectfully asserts that *Hoyt* does not teach the limitations of the new claims, either alone or in combination with any of the other cited references.

CONCLUSIONS

In view of the arguments advanced above, Applicant respectfully submits that claims 64-74 are in condition for allowance. Allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

EXPRESS MAIL LABEL NUMBER: EO 005 992 685 US
DATE OF DEPOSIT: 9/27/05
I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to Mail Stop , Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,

/E. Alan Davis/

By: _____

E. Alan Davis
Registration No. 39,954
Tel: (512) 301-7234

9/23/2005

Date: _____